Referring now to FIG. 3(*h*), a photoresist layer PR is deposited and patterned to open a window over the entire flash array. An arsenic implant A is performed at a dosage of about 5×10^{15} ions/cm^2 at 120 KeV at zero degrees to the normal to create the sources **12** and drains **13** of memory cells **10**.

Referring to FIG. 3(*i*), an arsenic implant A is performed at a dosage of about 3×10^{15} ions/cm^2 at 120 KeV, using photoresist PH to protect areas of the chip not implanted, to create the sources **12** and drains **13** of the low-voltage N-channel transistors LVT.

Referring to FIG. 3(*j*), a phosphorus implant P is performed at a dosage of about 4×10^{14} ions/cm^2 at 20 KeV, using photoresist PR to protect areas of the chip not implanted, to create the sources **12** and drains **13** of the high-voltage P-channel transistors HVT.

Referring to FIG. 3(*k*), the dopants of memory cells **10**, of low-voltage N-channel transistors LVT and high-voltage P-channel transistors HVT are driven with an anneal step at perhaps 900° C. for 20 minutes to complete formation of sources **12** and drains **13**. Oxide is deposited or grown and removed in conventional manner to form sidewall spacers SO.

A cap oxide (not shown) about 300 Angstroms thick is deposited over the surface. A borophosphosilicate glass (BPSG) layer (not shown) may then be deposited over the face of the slice. Following the BPSG deposition, the substrate **30** is heated again at about 900° C. for about one hour in an annealing ambient to provide BPSG densification, repair implant damage and junction profile drive. Column lines **18** and **25** are formed from a layer or aluminum after etching holes to sources **12** and drains **13** and other place on the chip where connection is desired. At the same time that column lines **18** and **25** are formed, other conductors are formed for logic circuitry. Off-array contacts for both memory and logic are masked and etched through the BPSG layer.

One problem with an isolated P-well **33** is high well resistance. The high well resistance causes a significant voltage drop during programming. The voltage drop is decreased by implant a P-type impurity P+ in the contact areas to P-well **33**. The contact areas should be strips, preferably extending along at least one side of each P-well **33**.

Metal is deposited, masked and etched to form metal lines to respective diffused regions, such as terminals **36** and **37** and the substrate terminal indicated Vdd. (The contact to P-well **33** may include a layer of previously-deposited doped polysilicon DP to decrease resistance.) This is followed by a protective overcoat process.

The invention described herein is usable with many other types of floating-gate memory cell arrays.

While the invention has been described with reference to an illustrative embodiment, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiment, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. it is, therefore, contemplated that the appended claims will cover any such modifications or embodiments that fall within the true scope of the invention.

We claim:

1. A method for making a nonvolatile, floating-gate memory with logic transistors in a face of a semiconductor body, comprising the steps of:

forming first and second opposite-conductivity-type diffusion regions having a first depth in said semiconductor body, said first and second opposite-conductivity-type diffusion regions doped to have primarily a second conductivity-type opposite said first conductivity-type;

forming first and second same-conductivity-type diffusion regions having a second depth in said semiconductor body, said first same-conductivity-type diffusion region encased in said first opposite-conductivity-type diffusion region, said second same-conductivity-type region separate from said first and second opposite-conductivity-type diffusion regions, said first and second same-conductivity-type diffusion regions doped to have primarily said first conductivity-type;

forming at least one floating-gate memory cell in and on said first same-conductivity-type diffusion region;

forming at least one high-voltage logic transistor in said second opposite-conductivity-type diffusion region; and

forming at least one low-voltage logic transistor in said second same-conductivity-type diffusion region.

2. The method according to claim **1**, wherein said semiconductor body is silicon of P conductivity-type, said first and second opposite-conductivity-type diffusion regions are primarily of N conductivity-type and said first and second same-conductivity-type diffusion regions are primarily of P conductivity-type.

3. The method according to claim **1**, wherein said first opposite-conductivity-type diffusion region and said first same-conductivity-type diffusion region are connected to a positive potential with respect to the potential of said semiconductor body during erasure of said floating-gate memory cell.

4. The method according to claim **1**, wherein Fowler-Nordheim tunnelling is used to program said floating gates of memory cells.

5. The method according to claim **1**, wherein said floating-gate memory cell is part of an X-cell memory array having single-dopant sources and drains.

6. The method according to claim **1**, further including formation of field oxide regions on the surface of said semiconductor substrate, said field oxide regions formed over the edges of said diffusion regions.

7. The method according to claim **1**, further including formation of field oxide regions on the surface of said semiconductor substrate, said field oxide regions formed over the edges of said diffusion regions and formed within said diffusion regions surrounding at least one connection point.

8. The method according to claim **1**, further including formation of field oxide regions on the surface of said semiconductor substrate, said field oxide regions formed to surround connection points to said diffusion regions, said first opposite-conductivity-type diffusion region and said first same-conductivity-type diffusion regions having multiple connection points at the periphery of said diffusion regions.

9. The method according to claim **1**, further including formation of diffused contacts in said first same-conductivity-type diffusion region, wherein said diffused contacts include additional doping of said same-conductivity-type.

10. The method according to claim **1**, further including formation of diffused contacts in said first same-conductivity-type diffusion region, wherein said diffused contacts are connected to doped polysilicon.

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